Topics: Non-destructive X-ray DiffractionTechniques for Analysis of Die Warpage and Stress Inside Fully Encapsulated Packaged Chips

Abstract:
To date there is no compelling metrology choice for the non-destructive measurement or imaging of stress/strain, warpage or defects inside Systems on Chip (SoC), Systems in Package (SiP) and other advanced integrated circuit packages. IN the past few years, Dublin City University has pioneered the use of a synchrotron-based technique using x-ray diffraction imaging (XRDI) combined with 3-dimensional surface modelling (3DSM) in order to enable such non-destructive metrology.

In this paper we will present recent advances in moving the technology away from synchrotron x-ray sources in order to demonstrate how a laboratory-based x-ray diffraction tool can be used to non-destructively image, map and measure Si strain/warpage inside packaged chips at various stages of the chip manufacturing process. Examples will be shown for micro-QFN and commercial QFN packages. Using a Jordan Valley Bede D1 high-resolution x-ray diffraction (XRD) system we have produced maps (x-ray spot size as small as 250 μm x 250 μm, fully encapsulated QFN chip scanned across the beam in 200 μm steps) of entire Si die up to 5 mm x 5 mm in dimension, which reveal warpage via mapping of rocking curve full widths at half maximum (FWHM) as a function of position. We will highlight data for two different approaches, namely (i) the use of ω scans or "rocking curves" [3] and (ii) the use of a series of spatially resolved line scans [4] across the sample under test. For the line scans the acquired data is reconstructed using a spline fitting and 3D surface model reconstruction technique outlined in reference [2].

These proof-of-concept laboratory-based tests confirm that one can easily highlight major warpage features non-destructively. Tilt and stress can also be evaluated separately from the FWHM data of the rocking curve maps. This development makes non-destructive imaging and evaluation of warpage/strain characterisation of Si wafer die inside packaged chips (throughout all process steps) using XRDI/3DSM in a fab setting a realistic possibility.